Docket No.: 10002929-3

AMENDMENTS TO THE CLAIMS

Claims 1-16 (Canceled)

17. (Previously Presented) Circuitry for providing external access to signals that are internal to an integrated circuit, said circuitry comprising:

a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit;

a trigger event generator receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on said sampled data based on said mask to provide a trigger event; and

a sampling circuit responsive to said trigger event to identify target data, wherein said sampling circuit includes switching circuitry configured to selectively provide a predetermined portion of said target data, wherein said predetermined portion of said target data is N/M bits wide where N/M is a positive integer.

- 18. (Previously Presented) The circuitry according to claim 17 wherein said sampling circuit includes multiplexing circuitry configured to combine M of said portions of said target data into a data unit N bits wide.
 - 19. (Canceled)

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Application No. 10/670,620 Amendment dated September 7, 2007 After Final Office Action of July 24, 2007

20. (Previously Presented) Circuitry for providing external access to signals that are internal to an integrated circuit, said circuitry comprising:

a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit;

a trigger event generator receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on said sampled data based on said mask to provide a trigger event; and

a sampling circuit responsive to said trigger event to identify target data, wherein said sampling circuit includes a FIFO storage array, and wherein said FIFO storage array is N/M bits wide where N/M is a positive integer.

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21. (Canceled)

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